



# UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,068	08/28/2001	Qiyong Bian	303.741US1	5646
21186	7590	10/19/2005	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH 1600 TCF TOWER 121 SOUTH EIGHT STREET MINNEAPOLIS, MN 55402			PHAN, THAI Q	
			ART UNIT	PAPER NUMBER
			2128	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/941,068	Applicant(s) BIAN, QIYONG	
	Examiner Thai Q. Phan	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2005.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☒ Claim(s) 21-30 is/are allowed.  
6) ☒ Claim(s) 1-20 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

This Office Action is in response to applicant's amendment filed on 07/28/2005.

Claims 1-30 are pending in the action.

#### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hekmatpour, Amir, US patent application publication no. 2002/01569292.

As per claim 1, Hekmatpour anticipates a method and system for interface of hardware and software for co-simulation and verification of a system on a chip with feature limitations similarly related to the claimed invention. According to Hekmatpour, the computer implemented method includes steps

Executing a client module configured to simulate behavior of an electronic system ([0037], [0038], [0043]),

Using a remote procedure call (RPC) to transfer process control ([0058]) to a server module that models behavior of a component of the electronic system ([0058]-[0062]),

Controllably advancing simulation time ([0077]), and

returning process control to the client module after execution of the server module ([0070]-[0077]) for the simulation.

As per claim 2, Hekmatpour anticipates Verilog/PLI module as claimed for design interface and verification processing ([0042]-0050)).

As per claim 3, Hekmatpour anticipated system C module ([0037]-[0050]).

As per claims 3-10, Hekmatpour anticipates the claimed limitations such as network protocol, sever, client, data transport layer, etc. for data communications and interfacing [0050]-[0070].

As per claim 11, Hekmatpour anticipates a method and system for interface of hardware and software for co-simulation and verification of a system on a chip with feature limitations similarly related to the claimed invention. According to Hekmatpour, the computer implemented method includes steps

Executing a client module configured to simulate behavior of an electronic system ([0037], [0038], [0043]),

Using a remote procedure call (RPC) to transfer process control ([0058]) to a server module that models behavior of a component of the electronic system ([0058]-[0062]),

Controllably advancing simulation time ([0077], and

returning process control to the client module after execution of the server module ([0070]-[0077]) for the simulation.

As per claim 12, Hekmatpour anticipates the client module is a Verilog/PLI module ([0037]-[0043]).

As per claim 13, Hekmatpour anticipates SoC or systemC module as claimed.

As per claims 14-20, Hekmatpour anticipates transport protocol for RPC, network data communication, component simulation, and interface for hardware/software co simulation as claimed.

### ***Allowable Subject Matter***

1. Claims 21-30 are allowed over the prior art of record. Following is examiner's statement reason for allowance.
2. The claimed invention is a computer implemented method and system with computer readable medium for Executing a Verilog/PLI module server configured to simulate behavior of an electronic system, using a remote procedure call (RPC) to transfer process control to a SystemC module that models behavior of a component of the electronic system, suspending operation of the SystemC module, advancing simulation time by one cycle of a clock signal having a 50% duty cycle, and returning a pointer associated with a return value to the Verilog/PLI module after the execution of the SystemC module.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent application publication no. 2002/0059054, issued to Bade et al, on May 2002

2. US patent application publication no. 2002/0170037 A1, issued to Powell, Edward, on Nov. 2002

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2128

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shah, K. can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oct. 12, 2005

  
Thai Phan  
Patent Examiner  
Art Unit 2128